JÜLICH
FORSCHUNGSZENTRUM

System-on-Chip (SoC)
Highly Integrated Solutions for Science

Nano- and Microelectronic Systems Group at ZEA-2

September 15th 2017| Carsten Degenhardt

Who is Carsten Degenhardt?

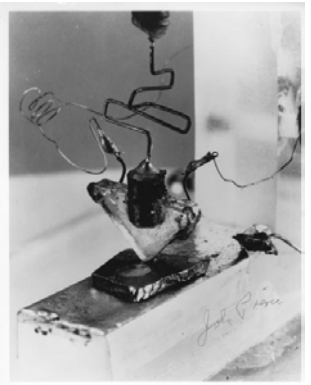
- 2001 Diploma in Solid-State Physics, Dortmund
- 2004 PhD in Quantum Optics, Hannover
- 2004-2008 Philips Research, Aachen
- 2008-2015 Philips Digital Photon Counting, Aachen
- 2015- ZEA-2, Head of Nano- and Microelectronic Systems, Research Center Jülich

Content

- Very Large Scale Integration (VLSI)
- Motivation to use VLSI for science applications
- Examples
  - Neutrino detector readout
  - Quantum Computing
- Outlook

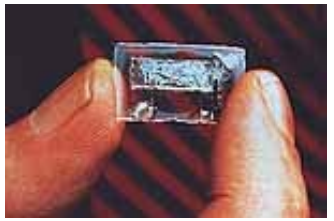
History of VLSI

- 1947: Transistor demonstrated by Shockley, Bardeen Brattain



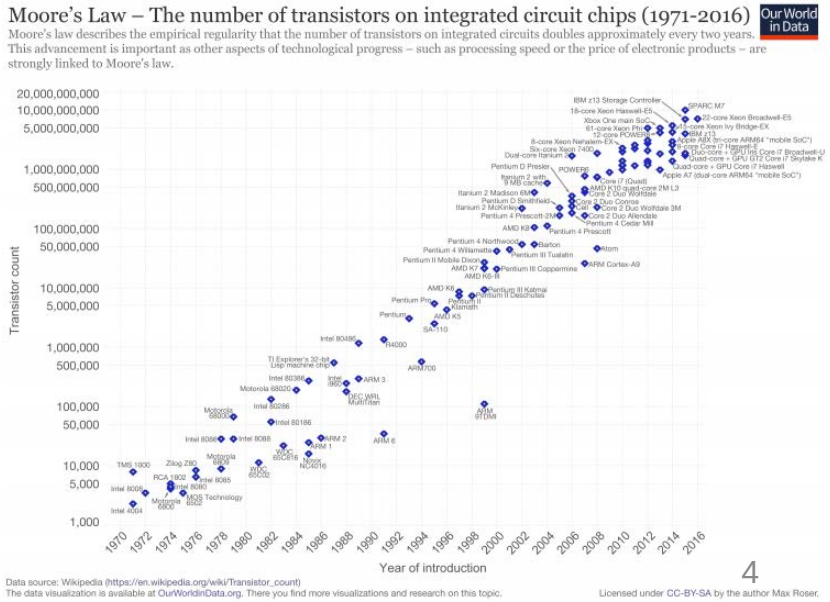
computerhistory.org

- 1950: the „Tyranny of numbers“ (Jack Morton, Bell Labs)



ti.com

- Late 1950s: Development of the ‚Integrated circuit‘ (Kilby, Noyce); many patent wars, since also others contributed (Hoerni, Jacobi, Dummer, …)



ourworldindata.org

- First microprocessor: Intel 4004, 1971

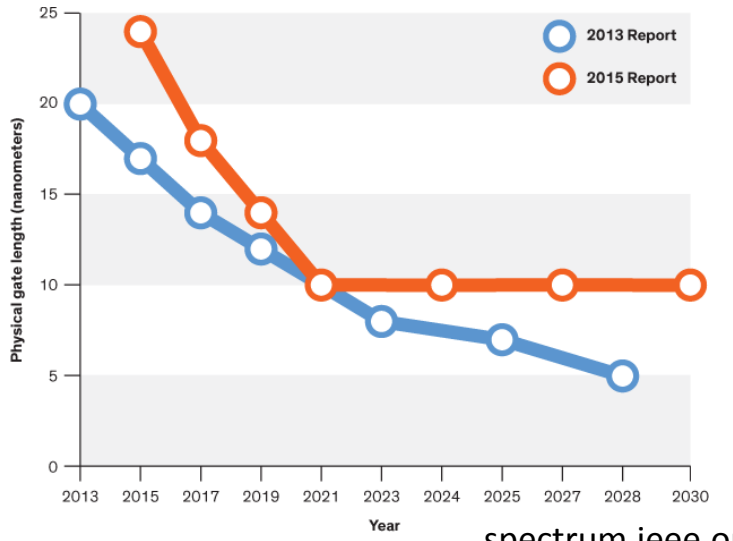
- Since then: Moore‘s law (doubling number of transistors every two years)

The power of large scale integration

- Process sizes reach 10nm for digital parts of the IC
- But: **analog electronics do not scale**
  (noise behaviour even gets worse with smaller processes)

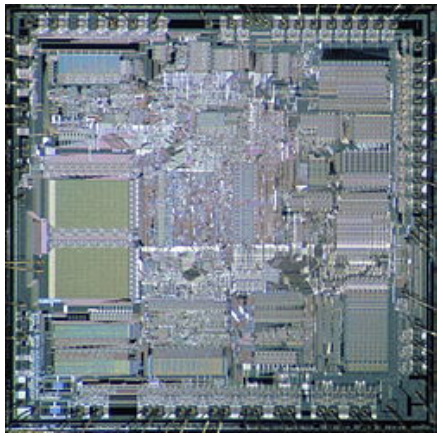
  ⇒ Do as much as possible in the **digital domain**

- Example: Ten 1pF capacitors need approx. 10.000 μm^2 chip area, With 28nm CMOS, 200.000 transistors can be placed in this area



spectrum.ieee.org

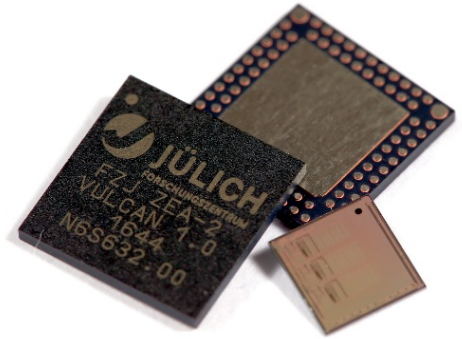
Intel 80286, 10x10mm^2, 134k transistors



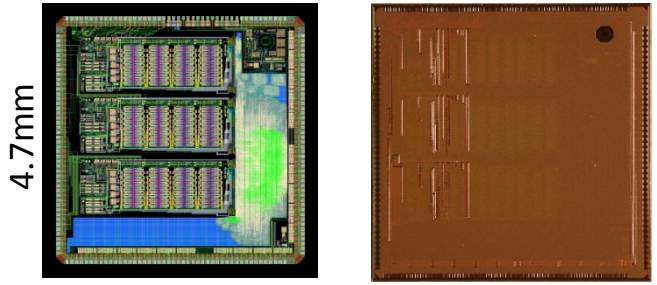
wikipedia.com

VLSI @ ZEA-2

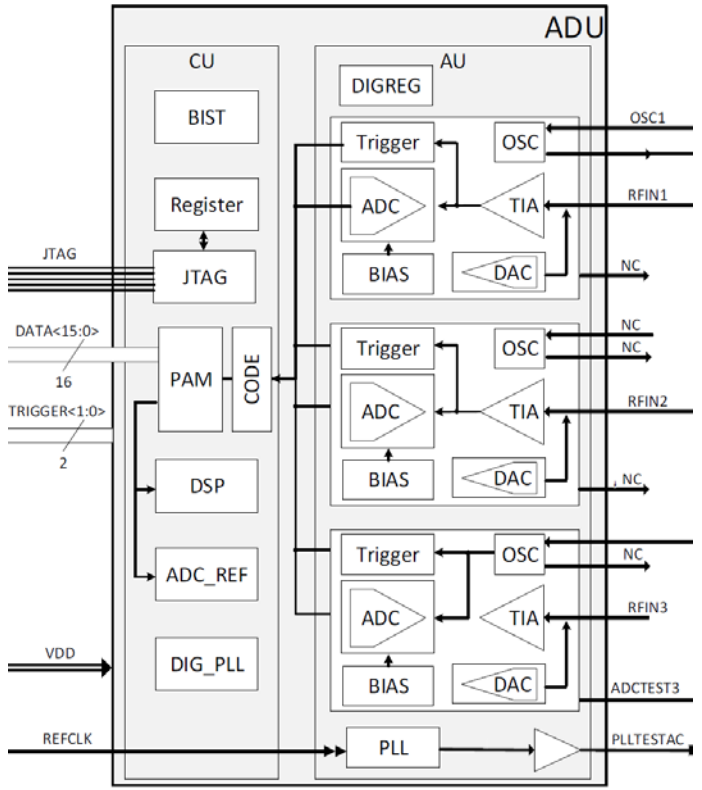
- **Today**
  - Development, testing and verification of highly integrated mixed-signal ICs
  - System Engineering
  - Platform creation



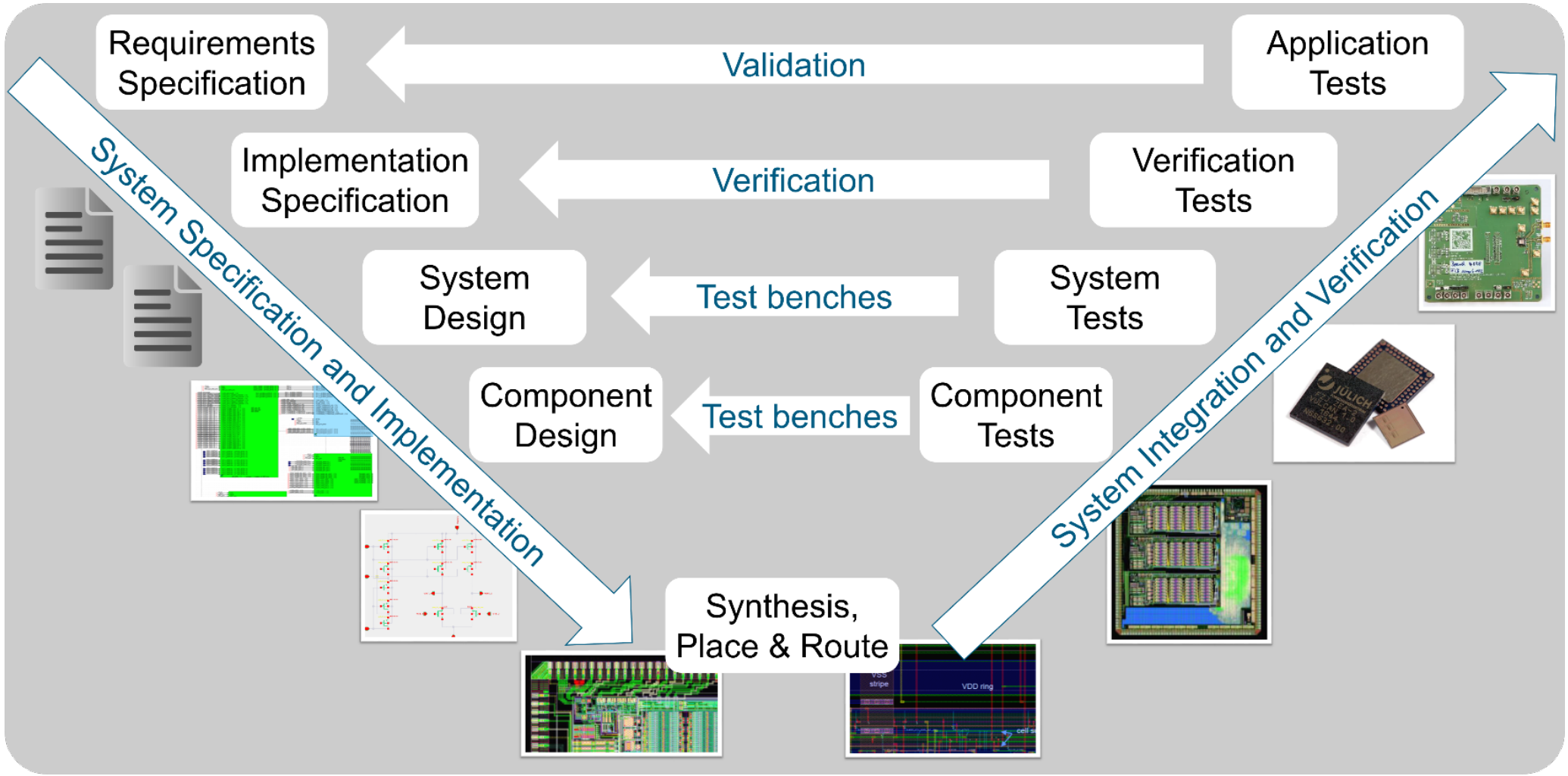
- **Tomorrow**
  - Embed more and more configurable intelligence into the chip
  - Include optical technologies (e.g. digital SiPM)
  - Low power, area efficiency, 3D packaging



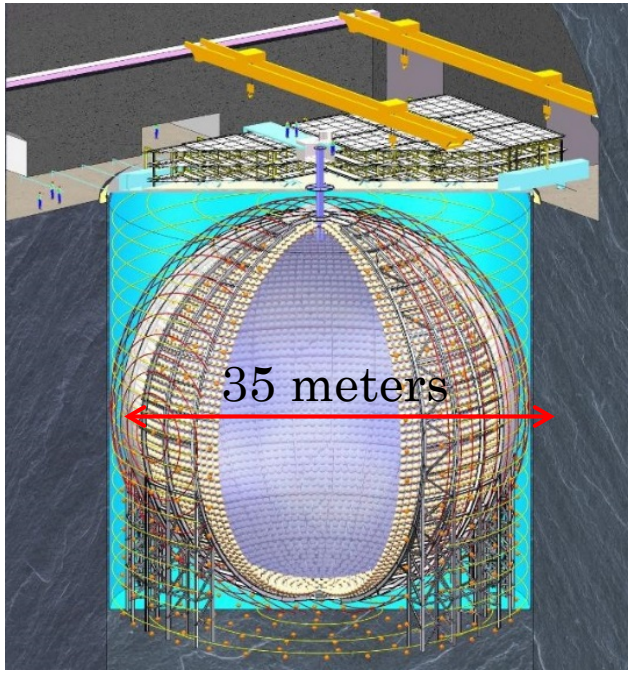
Prototype chip in TSMC 65nm



V-Model as a methodology for developing SoCs



Example: JUNO - Neutrino Observatory

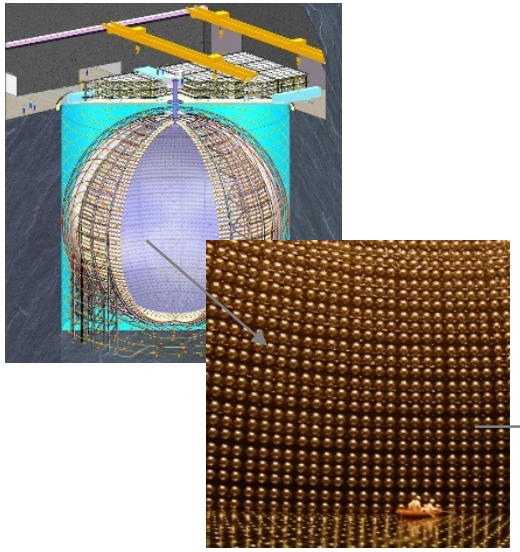


Central detector (700 m below ground level) [1]

Site of the Detector:
Close to Hongkong

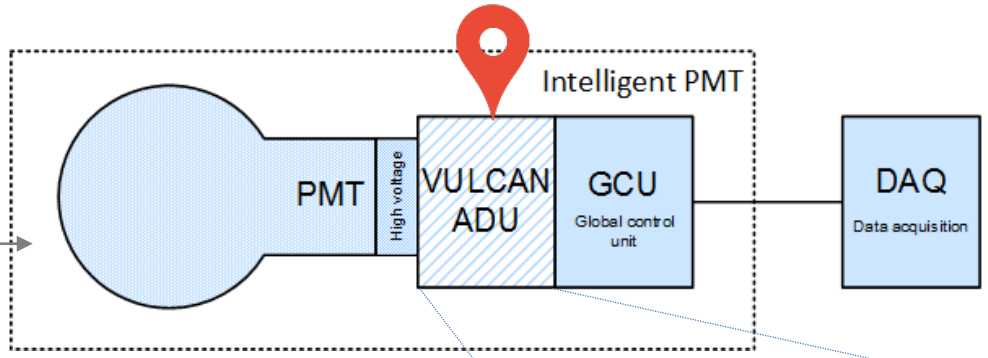
- Neutrinos are still a mystery:
  1. They are present everywhere
  2. They rarely interact
- Need for large specialized Neutrino detectors
- Usually build underground and filled with special liquid
- Jiangmen Undergound Neutrino Observatory (JUNO)
  1. Objectives:
     - Neutrino mass hierarchy
     - Search for Dark Matter
     - Study of Supernova explosions
  2. Constructed 700 meters below ground (natural barrier acts as filter)
  3. 64 Institutes and Universities, 12 Countries, >400 Researchers

ZEA-2 Involvement in JUNO



Interior of a detector[3]

Single Photomultiplier[4]

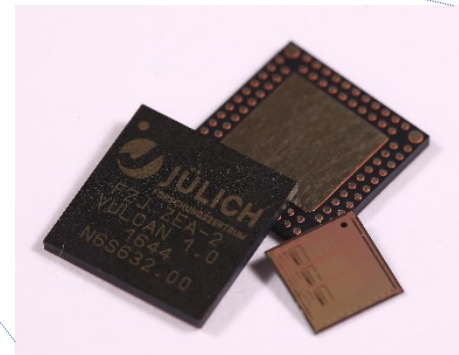


Photomultiplier tube with electronics

Photomulitplier tubes: Photons to current

Q: What next ?
Store the signal for analysis

Q: How do we do that ?
1. Convert the current to voltage
2. Digitize the signal (Analog signal to digital signal)



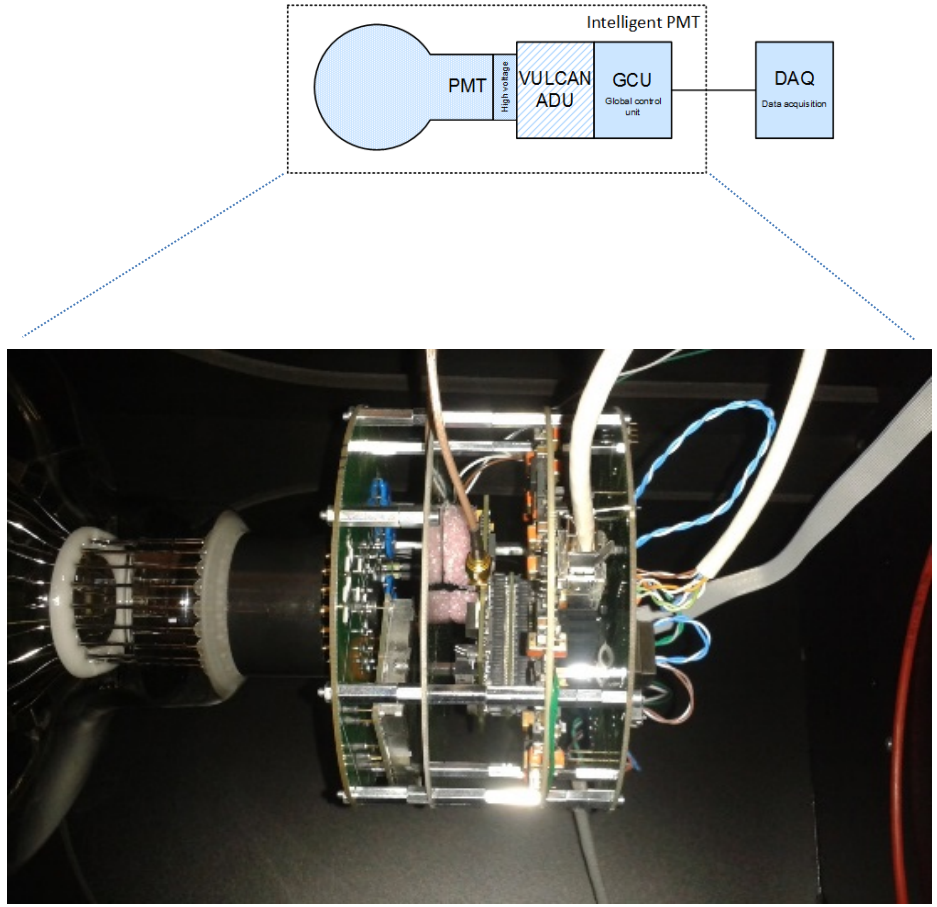
Vulcan first prototype

Vulcan – Closer view

A Highly integrated circuit placed closed to the PMT prevents signal loss and preserves the signal integrity.

Vulcan - Key features:

- Parallel Analog to Digital converters to achieve good resolution for a large input range
- Low power consumption
- Dedicated control unit for data processing
- Various modes of operation
- High configurability for gain selection, operations performed on data and others



Electronics connected to the base of PMT[5]

VULCAN Details

Three ADCs with 1GS/s, Trans-Impedance-Amplifiers with variable gain to achieve large dynamic range

- Selection of best resolution data from three ADCs
- Data reduction and compression (noise data)

  Input : 24 bit × 1 GHz = 3 Giga Bytes/s

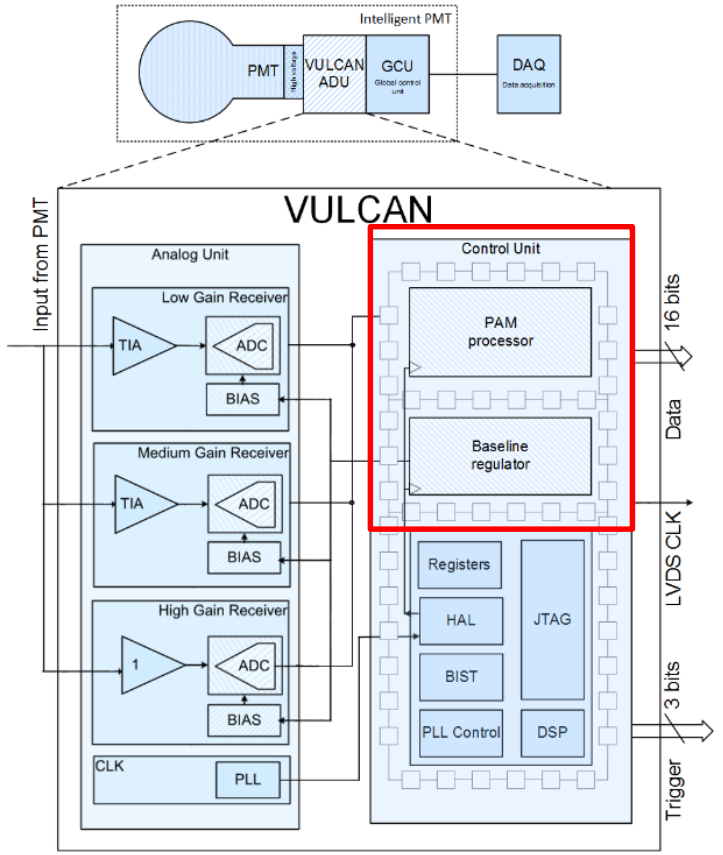
  Output : 16 bit × 500 MHz = 1 Giga Bytes/s

Baseline regulator

- Biasing fluctuation and intersymbol interference shift the baseline
- Unregulated ADC output indicates a different charge than the actual input

Design for Test

- Scan chain insertion for identifying manufacturing defects
- Increasing test access points without tremendously increasing input & output pins



Vulcan Overview

Example: Quantum Computing

Classical bits
0 or 1

N bits => 2^N states 0, 1, …, 2^N-1

Quantum bits (qubits)
$\alpha|0\rangle + \beta\ |1\rangle$

N qubits: 2^N dimensional Hilbert space $|0\rangle$, $|1\rangle$, …, $|2^N\text{-}1\rangle$
Superposition of states, Entanglement

Make use of the principles of quantum mechanics

⇒ Built-in parallelism

⇒ Exponential speedup (for some problems)
- ⇒ Protein folding (drug development)
- ⇒ Catalyst research (efficient fertilizer production)
- ⇒ Cryptography (secure communications)

Qubit representations

There are a lot of physical possibilities to represent a qubit:

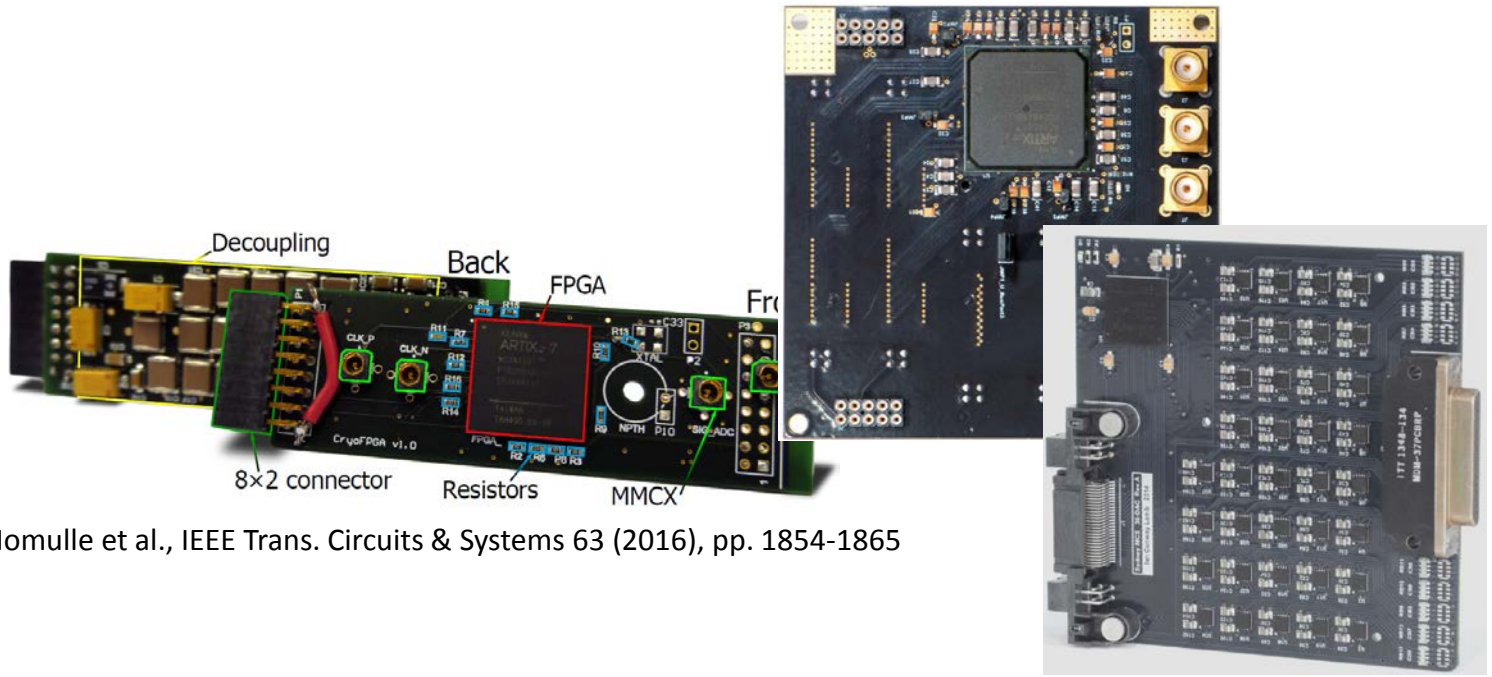
- Photons (Polarization)
- Ions (Atomic states)
- Spins (Nuclear, Electron)
- Josephson junctions (Charge, flux)
- Quantum Dots (Charge, Spin)

Promising candidates are solid state qubits using electron spins (GaAs, Si)

- Easy to manufacture (lithography)
- Easy control (electrical pulses)
- Potential of high integration

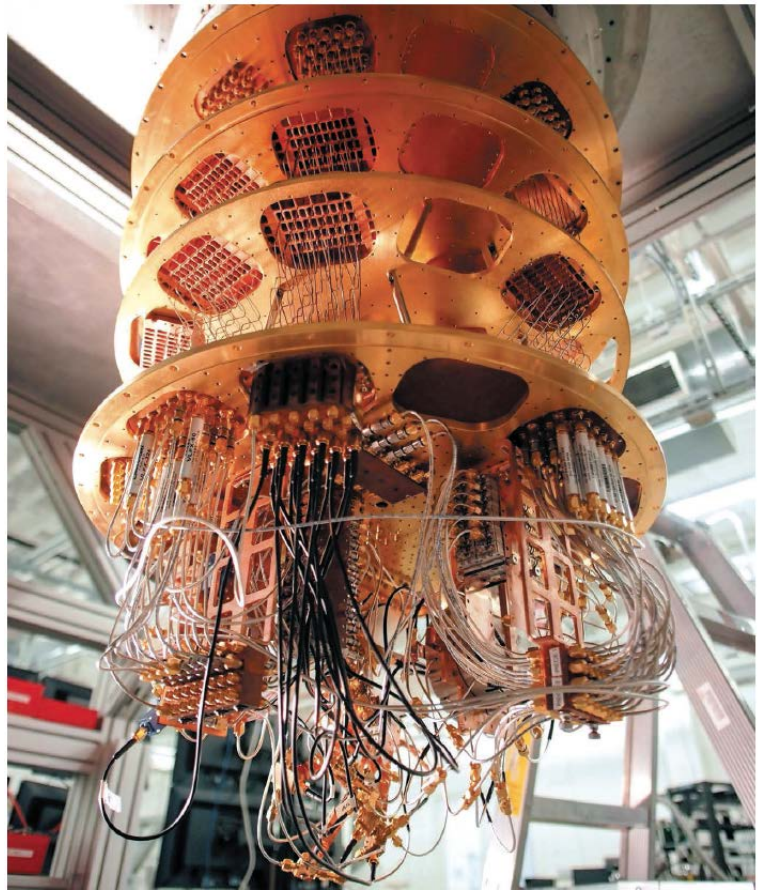
Control Electronics for Quantum Computers

- ‘Brute force’ scaling to operate up to 50-100 qubits
- Further scaling very difficult



Homulle et al., IEEE Trans. Circuits & Systems 63 (2016), pp. 1854-1865

Lamb et al., Rev. Sci. Inst. 87 (2016), pp. 1-7



Mohseni et al., Nature 543 (2017), pp. 171-173

Control Electronics for Quantum Computers

Goal

- Design, implement and test scalable control electronics for quantum computers

Challenges

- Scalability (area, power consumption, interface)
- Cryogenic environment with very limited cooling power (few Milliwatts in total at < 100mK)
- Area restrictions for 1:1 coupling of electronic with qubits
- Interface to room temperature electronics

→ **Only possible with dedicated highly integrated circuits**

Dilution refrigerator
oxford-instruments.com

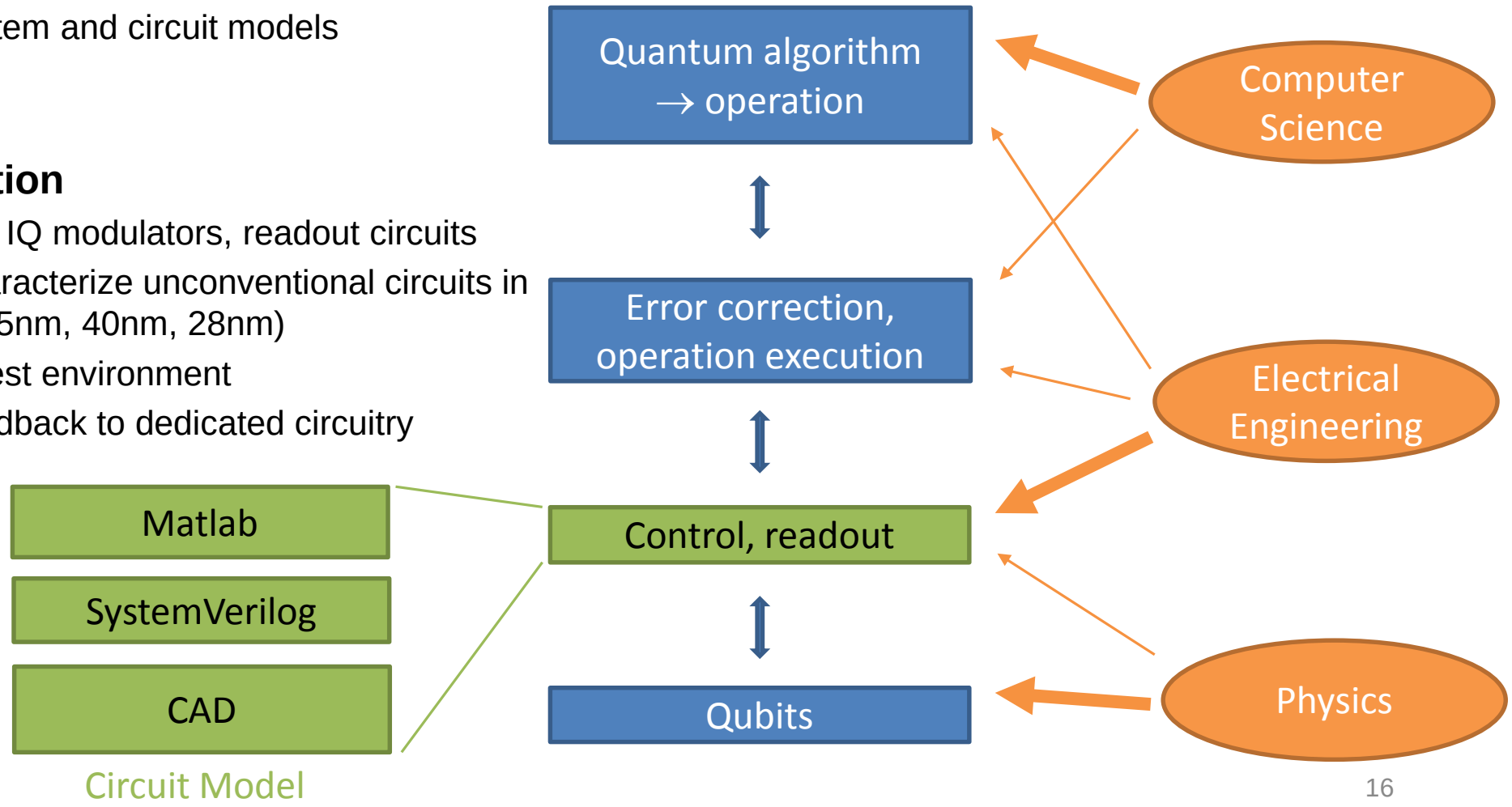
Control Electronics for Quantum Computers

Top-Down Design

- Define interfaces and specify requirements
- Parameterized system and circuit models (system modeling)

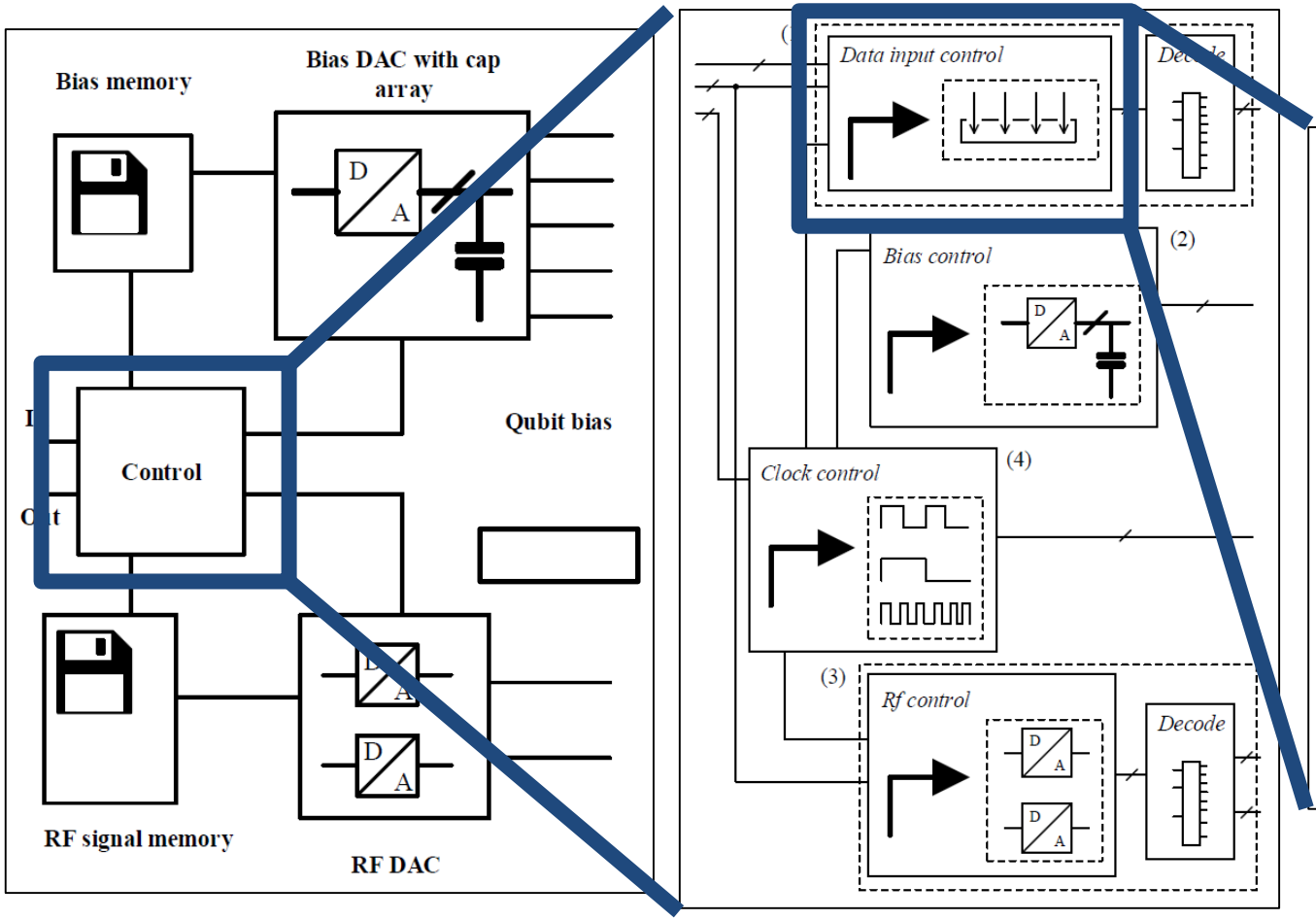
Bottom-Up Implementation

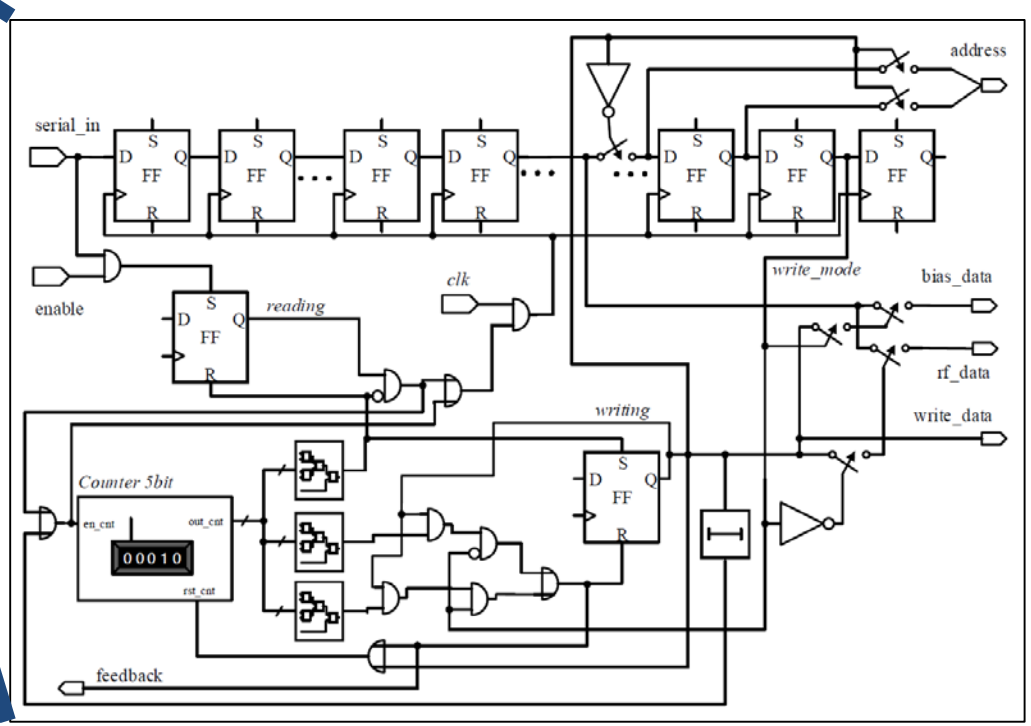
- DC DAC, AC DAC, IQ modulators, readout circuits
- Implement and characterize unconventional circuits in standard CMOS (65nm, 40nm, 28nm)
- Set-up cryogenic test environment
- Refine models; feedback to dedicated circuitry development



System Design

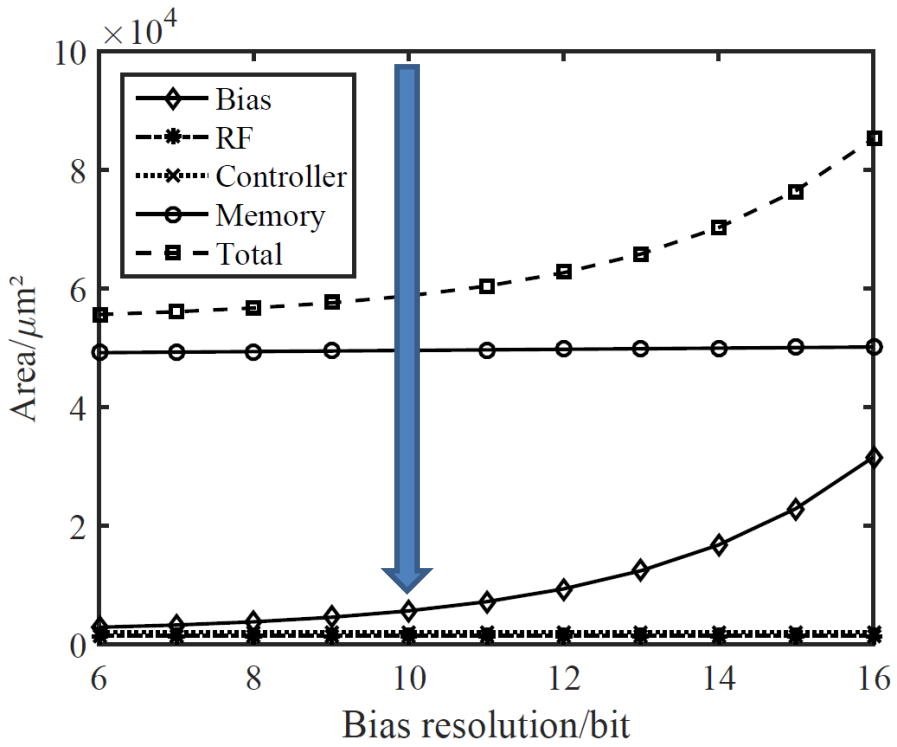
Top-down system decomposition into individual components (down to transistor level)

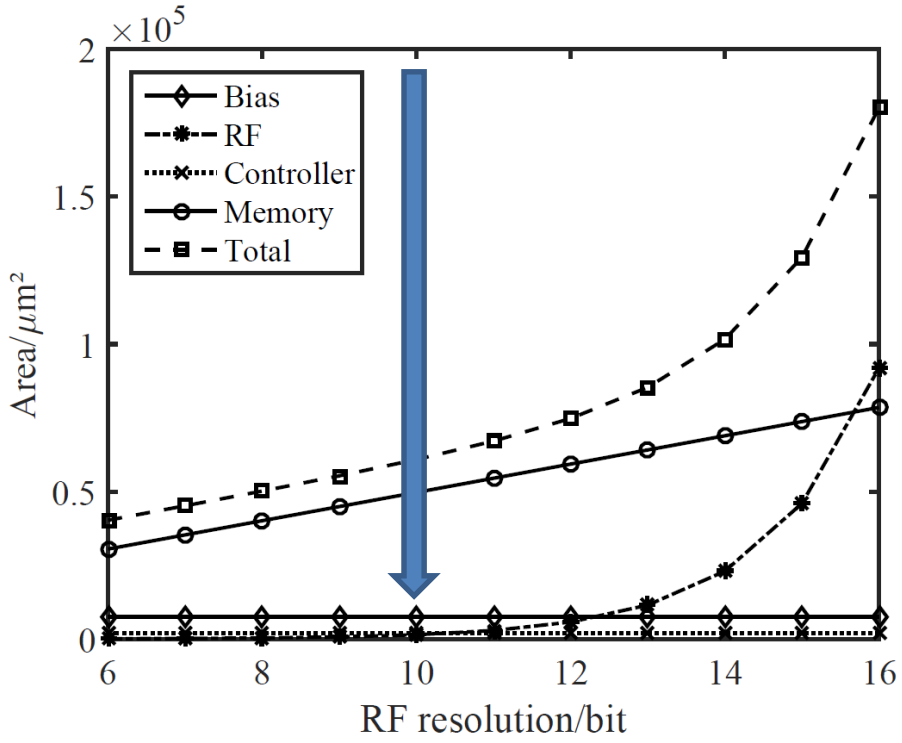




Area Demand

Estimated for standard 65nm CMOS process, no optimization taken into account yet



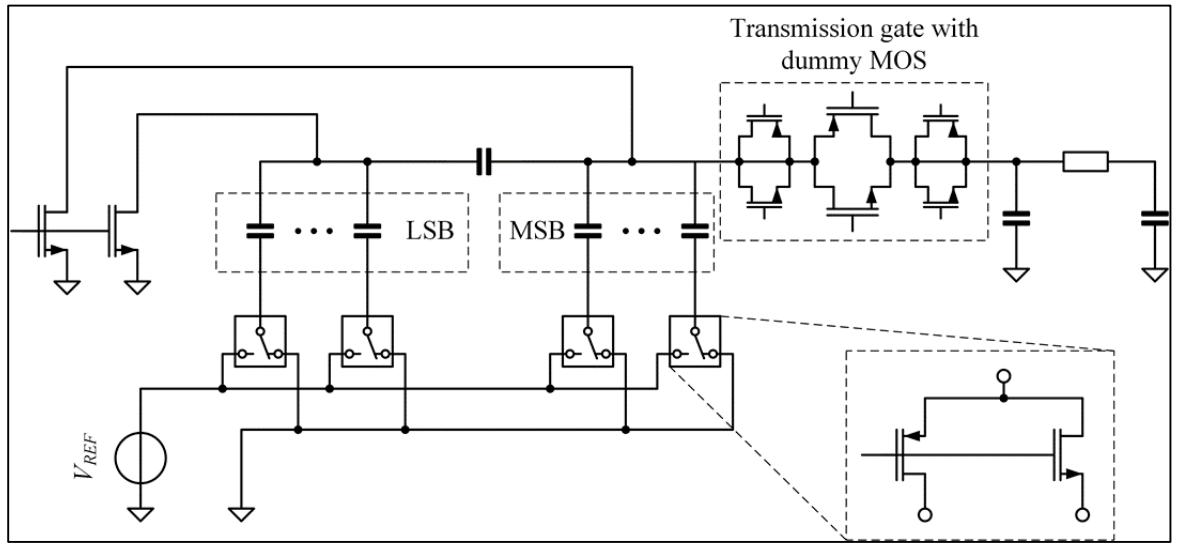


Approx. 60000 μm² (250 x 250 μm²) control electronics for one qubit

Power Consumption

- Use of unconventional approaches to reduce power consumption

Charge-division DAC



10 qubits could be operated with cooling power of 1mW

Component	Power consumption @ V_{dd}=1V
DAC	< 20μW
Memory	3 μW
Control	50 μW
Total	**< 100 μW**

Outlook: Generic Readout Platform

Motivation

- Detector systems become more and more complex
  → IC designs become more and more complex (labor, time → cost)
- There are only few examples where specific ICs could be reused

Approach

- Develop a generic, scalable and flexible front-end readout architecture
- Make use of large scale integration technology

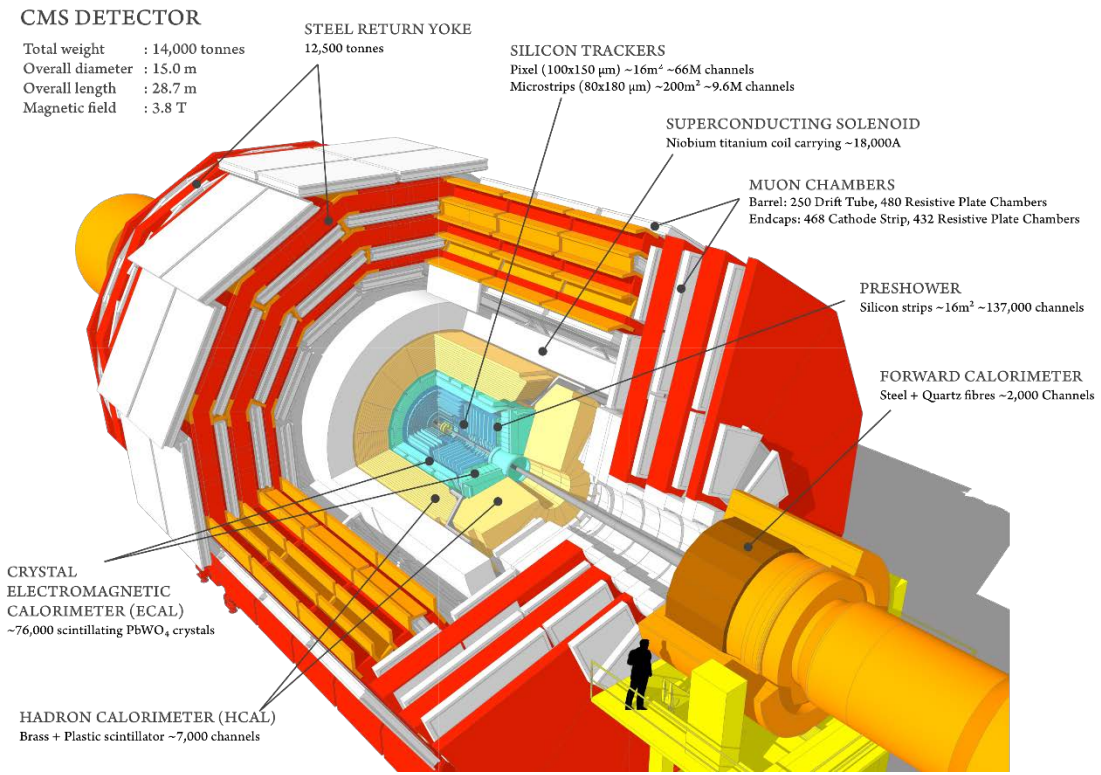
Benefits

- Allows a faster system integration into multiple applications
- Shorter development cycles
- Unified interfaces
- Reuse of existing hardware, firmware, software
- Less resources needed compared to dedicated developments
- Opens up new possibilities with respect to performance and flexibility
- Smaller form-factor
- Easier detector upgrades
- Upgrades directly benefit from advancements in large scale integration technology
- Easier (less time consuming) maintenance

Detector example CMS@LHC

- Collaboration has 4300 active people
- Approx. **40 different ASICs used** in CMS

- Inner tracker (76M channels, **silicon-pixel and silicon-strip**)
  - Readout ASIC bump bonded to detector (96.000 ASICS)
  - Signal transmitted by 40.000 fiber links
- ECAL (electromagnetic calorimeter)
  - 76.000 PbWO4 scintillation crystals (2x2x23cm^3, 3x3x22cm^3)
  - +/- 0.1K temp stabilization, water cooling
  - **APD and VPT** (vacuum photo triodes) used for light detection
  - Signals transmitted by optical Gb links
- HCAL (hadron calorimeter)
  - Brass+ plastic scintillators, wavelength-shifting-fiber readout to **HPDs** (hybrid photodiodes)
  - 7000 channels
- Muon detector
  - 180.000 **drift tubes**
  - Readout ASIC 'The MAD': charge preamplifier, shaper, baseline restorer; latched discriminator; LVDS output; 80.000 ASICs needed; 25mW per channel

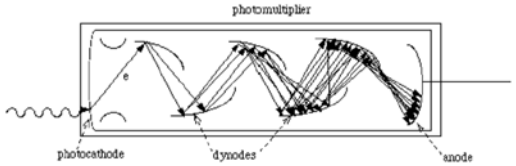


CMS-Collaboration. (2006). *CMS Physics - Technical Design Report, Volume I.* Geneva: CERN.

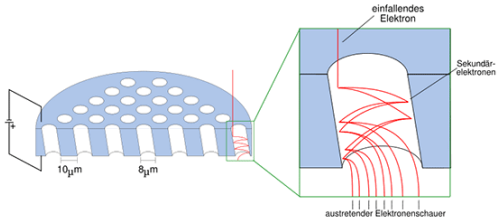
Readout requirements for different detector types

Property	Light detectors	Gas based detectors	Pixel/strip detectors
Signal amplitude	O(nC)	O(pC)	O(fC)
Detector capacitance	O(pF)	O(pF)	O(fF)
Noise	O(1.000 e- rms)	O(1.000 e- rms)	O(100 e- rms)
Number of channels	O(10E5)	O(10E6)	O(10E8)
Radiation hardness	O(0.5 Mrad)	O(0.01 Mrad)	O(10 Mrad)

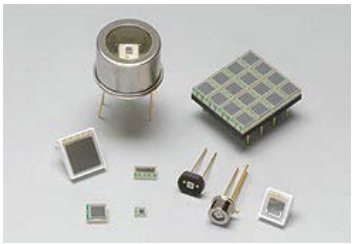
Photomultiplier tubes

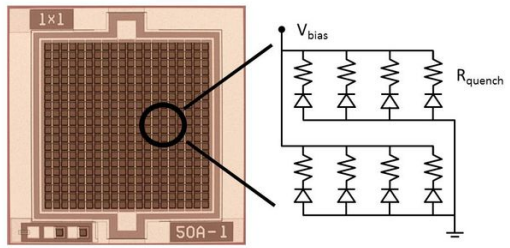


Microchannel plates

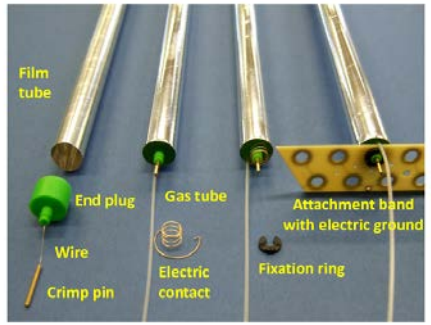


Silicon based light detectors

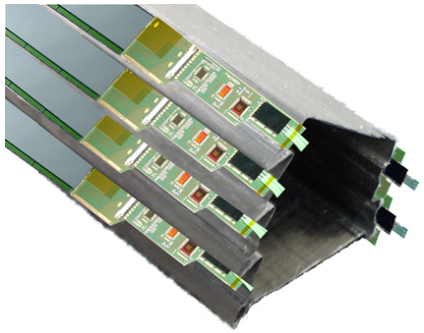




Gaseous detectors



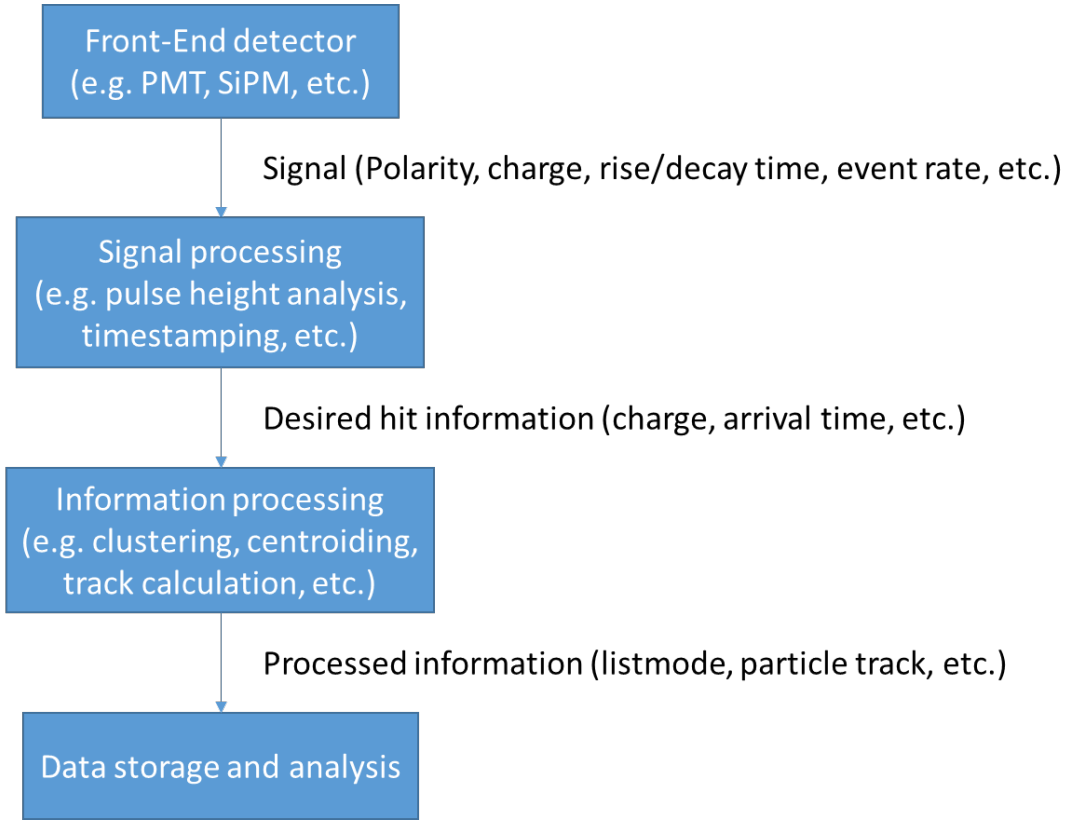
Silicon pixel/strip detectors



Scalable readout platform

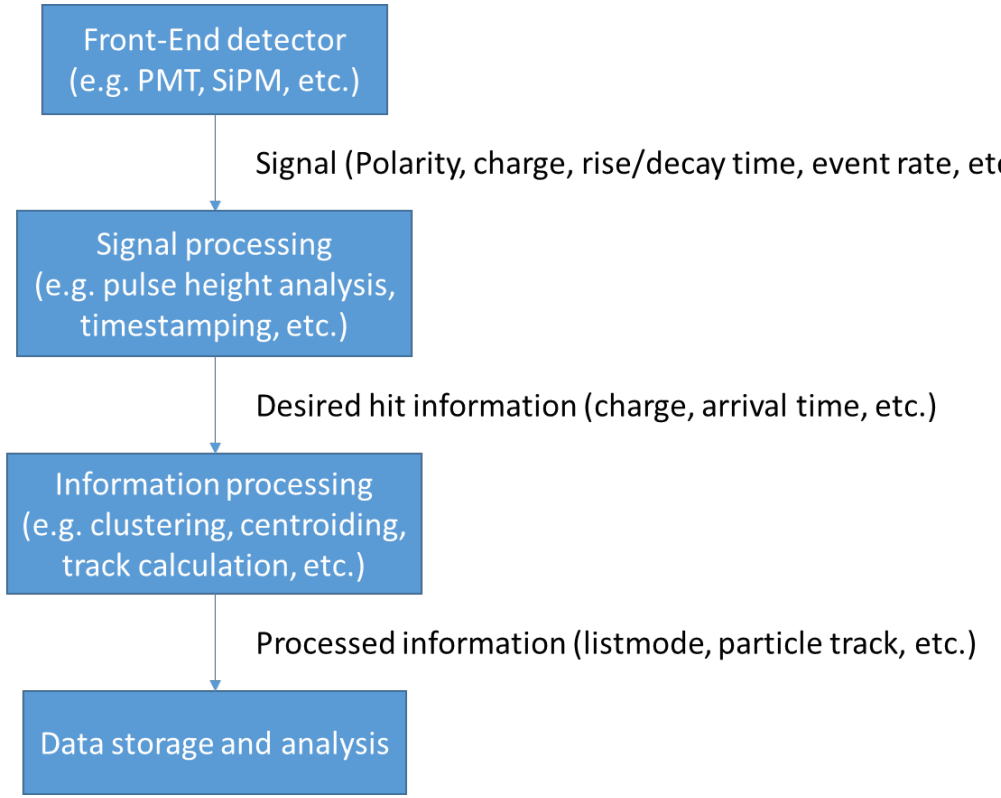
Problem: Chip development is expensive (time, effort, material)

Solution: Develop scalable and flexible implementation to share development costs between multiple applications



Signal processing

- (Multiple) thresholding
- Trigger generation
- Timestamping
- Determination of pulse integral
- Baseline tracking and restoration
- Tail cancellation
- Pile-up detection (and correction)
- Temporary storage of data
- Statistics gathering (rates, dead time)



- Benefits of digital pulse processing
- Imperfections of the ADC (like non-linearity) can be corrected for by the digital part of the front-end
- Signal processing can be done digitally in a programmable manner

Summary

- There is tremendous potential in using large scale integration for scientific challenges
- Constant miniaturization of feature sizes allows to put more and more tasks into the digital part of the circuits
- High development costs require flexible and scalable approaches to serve multiple applications


Thank You!
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